18ELN14/24
USN


# First/Second Semester B.E. Degree Examination, July/August 2021 Basic Electronics 

Time: 3 hrs .
Max. Marks:100

## Note: Answer any FIVE full questions.

1 a. Explain the operation of $\mathrm{p}-\mathrm{n}$ junction Diode under unbiased condition with a neat diagram.
(08 Marks)
b. In a full wave rectifier, input is from $30-0-30 \mathrm{~V}$. The load and $\mathrm{R}_{\mathrm{f}}$ are $100 \Omega$ and $10 \Omega$ respectively. Calculate area voltage, efficiency, percentage regulation.
(06 Marks)
c. Determine $\mathrm{I}_{\mathrm{D}}, \mathrm{V}_{1}, \mathrm{~V}_{2}$ and $\mathrm{V}_{0}$ for the given circuit.


Fig.Q1(c)
(06 Marks)
2 a. With a neat diagram and waveforms explain the working of a bridge rectifier.
(08 Marks)
b. Explain the operation of a zener diode with line regulation and load regulation.
(08 Marks)
c. For a zener regulator shown in Fig.Q2(c), calculate the range of input voltage for which output remain constant. $\mathrm{V}_{\mathrm{Z}}=6.1 \mathrm{~V}, \mathrm{I}_{\mathrm{Z} \min }=2.5 \mathrm{~mA}, \mathrm{I}_{\mathrm{Z} \max }=25 \mathrm{~mA}, \mathrm{r}_{\mathrm{Z}} \Rightarrow 0 \Omega$.

(04 Marks)
3 a. Explain the characteristics of N-channel JFET(Drawn and transfer characteristics).(12 Marks) b. For a N -channel JFET, $\mathrm{I}_{\mathrm{DSS}}=8 \mathrm{~mA}, \mathrm{~V}_{\mathrm{P}}=-5 \mathrm{~V}$. Find :
i) $\mathrm{I}_{\mathrm{D}}$ @ $\mathrm{V}_{\mathrm{GS}}=-2 \mathrm{~V}$ and -3 V
ii) $\mathrm{V}_{\mathrm{GS}} @ \mathrm{I}_{\mathrm{D}}=3 \mathrm{~mA}$ and 5 mA .
(06 Marks)
c. List out classification of FET with symbols.
(02 Marks)
4 a. Draw and explain forward and reverse characteristics of an SCR.
(07 Marks)
b. Sketch the transfer and drain characteristics for an n-channel depletion - type MOSFET for the range of values of $\mathrm{V}_{\mathrm{GS}}=-6 \mathrm{~V}$ to +1 V with $\mathrm{I}_{\mathrm{DSS}}=8 \mathrm{~mA}, \mathrm{~V}_{\mathrm{P}}=\mathrm{V}_{\mathrm{GS}(\text { off })}=-6 \mathrm{~V}$.
(08 Marks)
c. With a neat diagram, explain the 2 transistor model of SCR.

5 a. Explain following with respect to OP-Amp.
i) Virtual ground
ii) CMRR
iii) Slew rate
iv) Offset voltage
v) Matched transistors.
(10 Marks)
b. Derive the expression for output voltage of an
i) integrator
ii) inverting summing amplifi

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18ELN14/24

6 a. Explain the ideal characteristics of on op-Amp.
(08 Marks)
b. Derive the expression for output voltage of an non inventing amplifier with a neat circuit and waveform.
(08 Marks)
c. Design an adder circuit using an op-Amp to obtain output expression. $\mathrm{V}_{0}=-2\left(0.1 \mathrm{~V}_{1}+0.5 \mathrm{~V}_{2}+20 \mathrm{~V}_{3}\right)$.
(04 Marks)
7 a. Explain the operation of BJT as an amplifier and as a switch.
(10 Marks)
b. Draw and explain the operation of a voltage series -ve feedback amplifier and derive an expression for its input impedance.
(10 Marks)
8 a. Define an oscillator. Explain Brakhausen's criteria for oscillations with block diagram.
b. Derive the expression for frequency of oscillations of Wien bridge oscillator.
(06 Marks)
c. With a neat diagram, explain the working of RC phase shift oscillator.

9 a. Subtract $(111001)_{2}$ from $(101011)_{2}$ using 2's complement method.
(04 Marks)
b. State and prove Demorgan's theorem for 3 variables.
(04 Marks)
c. Simplify the following Boolean expression :
i) $\mathrm{A}+\overline{\mathrm{A}} \mathrm{B}=\mathrm{A}+\mathrm{B}$
ii) $\bar{X} \bar{Y} \bar{Z}+\bar{X} \bar{Y} \bar{Z}+\bar{X} \bar{Y}+X \bar{Y}$
iii) $\overline{\overline{X Y}+X Y Z}+X(Y+X \bar{Y})$
iv) $\mathrm{ABC}+\mathrm{A} \overline{\mathrm{B}} \mathrm{C}+\mathrm{AB} \overline{\mathrm{C}}+\overline{\mathrm{ABC}}$
v) $\mathrm{A} \overline{\mathrm{B}}+\mathrm{ABC}+\mathrm{A}(\mathrm{B}+\mathrm{A} \overline{\mathrm{B}})$
vi) $\mathrm{AB}+\overline{\mathrm{AC}}+\mathrm{A} \overline{\mathrm{B}} \mathrm{C}(\mathrm{AB}+\mathrm{C})$.
(12 Marks)
10 a. With block diagram and truth table, explain the operation of full ladder using 2 half adder.
(08 Marks)
b. Explain the operation NOT, AND and OR gates using analogous switch equivalent circuit.
(09 Marks)
c. Implement Ex - OR gate using only NOR gate.

